

High End Computing Research & Development

SC2002 HEC BOF 19 November 2002

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NSA's High End Computing R&D Program

HEC Architectures and Systems
Collaboration with DARPA on HPCS
High Speed Switches and Interconnects
Superconducting Electronics
Thermal Management
Programming Environments
Quantum Information Sciences



The Pervasive Architectural Issue

Type T Systems*

Commodity Components, Sub-systems

Performance: Degrades with Scaling

Server Architectures (SMP)

4-128 Processor

Relatively High Latency

Distributed Memories (Shared in Node)

Memory BW: Poorer

Programming Model: Usually MPI

Programmability: Harder

Initial Cost: Less

Type C Systems*

Highly Customized

Performance: Better Sustained

Various Architectures (MPP, PVP...)

8-128 Processors/Node

Accelerators: Vector, Multithreading

Registers, Special Functions

Distributed, Shared Memories

Memory BW: Better

Programming Model: Shmem, MPI

Programmability: Easier

Initial Cost: More



CRAY X1





CRAY X1

- Multi-year Joint Development Effort in Scalable Vector Architecture
- Technology Transfer NSA Developed Technology
- Aug-Sept '02: Prototypes delivered
- Production Model Delivery by Year's End
- Collaboration with DoD/DDRE
- Joint Development Program Continues on X1e and Next Generation System



HAC Task on HEC R&D Program

- Multi-agency Study Resulted in Development and Acquisition Plan for HEC R&D Program
- Participants:
 - Executive panel: NSA, DUSD S&T, DoE
 - Agencies conducting R&D in HEC for national security applications: NSA, DARPA, NNSA, NASA
 - National Security users of HEC: NSA, NNSA, NASA, DoD
 High Performance Computing Modernization Program, ASD
 C3I, Naval Oceanographic (Fleet Numerical), NIMA, NRO,
 military high end computing laboratories
- Status: Study in DoD; Coordination & Funding



HEC Needs for National Security

- Comprehensive Aerospace Vehicle Design
- Operational Weather/Ocean Forecasting
- Stealthy Ship Design
- Nuclear Weapons Stockpile Stewardship
- Army Future Combat Systems
- Weapons Development
- Intelligence Support
 - Imagery & Geospatial Intelligence
 - Signals Intelligence
 - Threat Weapons Systems Characterization



HEC Improvements Needed

- Sustained Performance: 4-100X
- Scalable, Balanced Architectures
 - Interconnects (Processor, Memory, Board, Node)
 - Larger, Global Shared Memories
 - Scalable I/O
 - Processor Designs
 - Systems Software
- Reduction in Power & Size
- Improved Cooling
- Programming Paradigms
- Ease of Use (Tools, Tools, Tools)
- Time to Solution